Pixel Array Detectors (PADs) & Analog Examples

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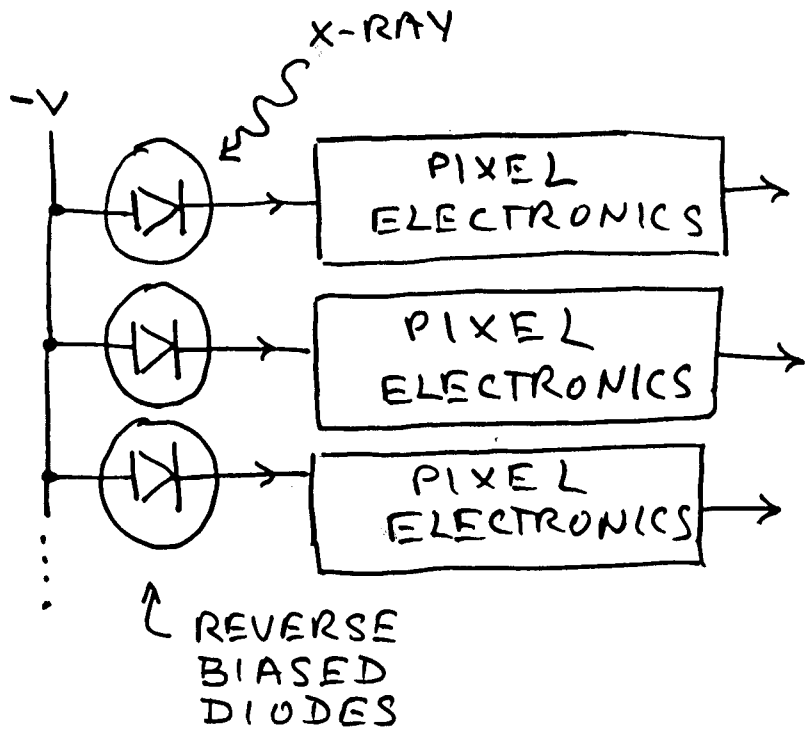
Talk Outline

1) General introduction to PADs.

2) Recent work on analog PADs

What is a PAD?

1) Each pixel has it own electronics.
2) Direct conversion of X-rays to electrical signals in the pixel.



3) ~~To maximize fill-factor and stopping power, while still utilizing standard CMOS foundry fabrication, many PADs are two layer devices.~~

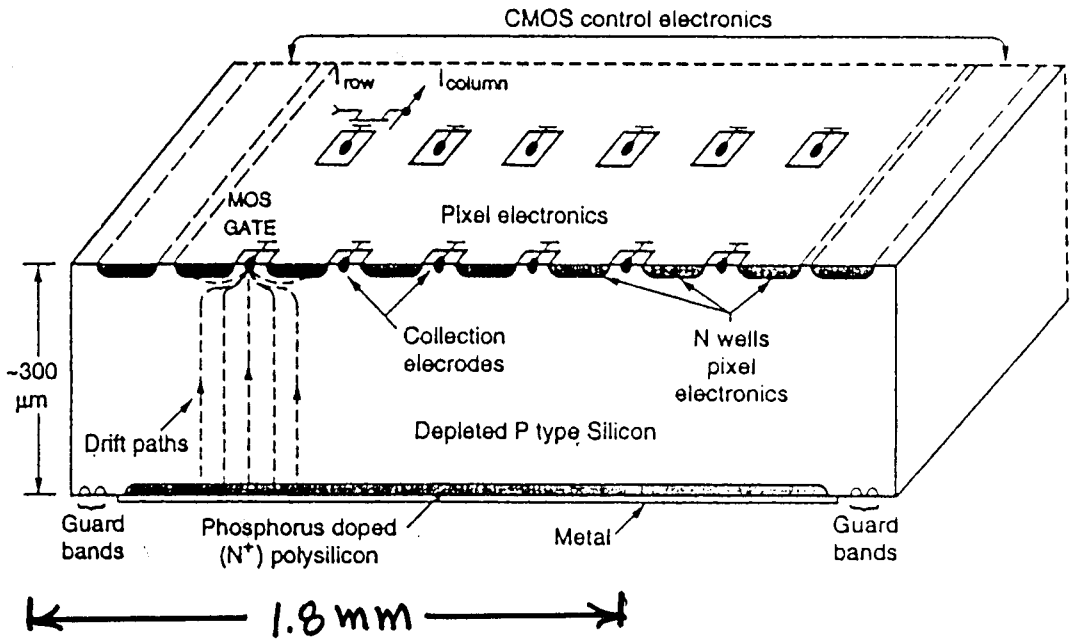
1460

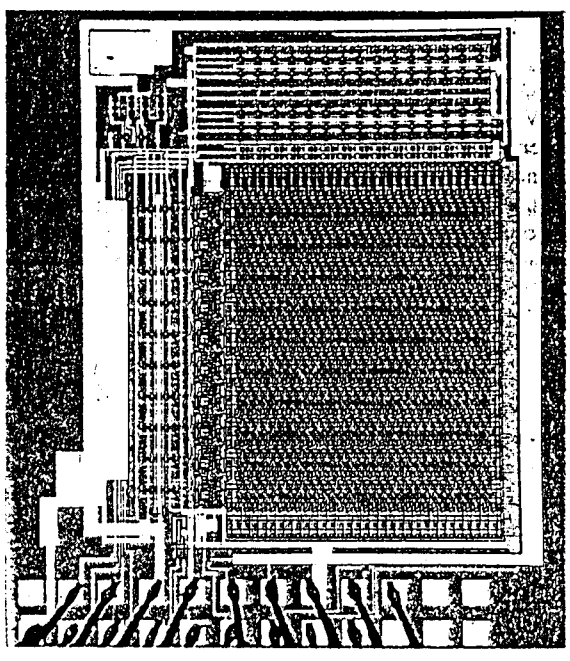
NIM A326 (1993) 144–149

First beam test results from a monolithic silicon pixel detector *

Walter Snoeys, James Plummer, Geert Rosseel and Chye Huat Aw
Center for Integrated Systems, Stanford University, Stanford, CA 94305, USA

Chris Kenney and Sherwood Parker
University of Hawaii, Department of Physics, High Energy Physics Group, Honolulu, HI 96822, USA





30 × 10 PIX

2.2 mm

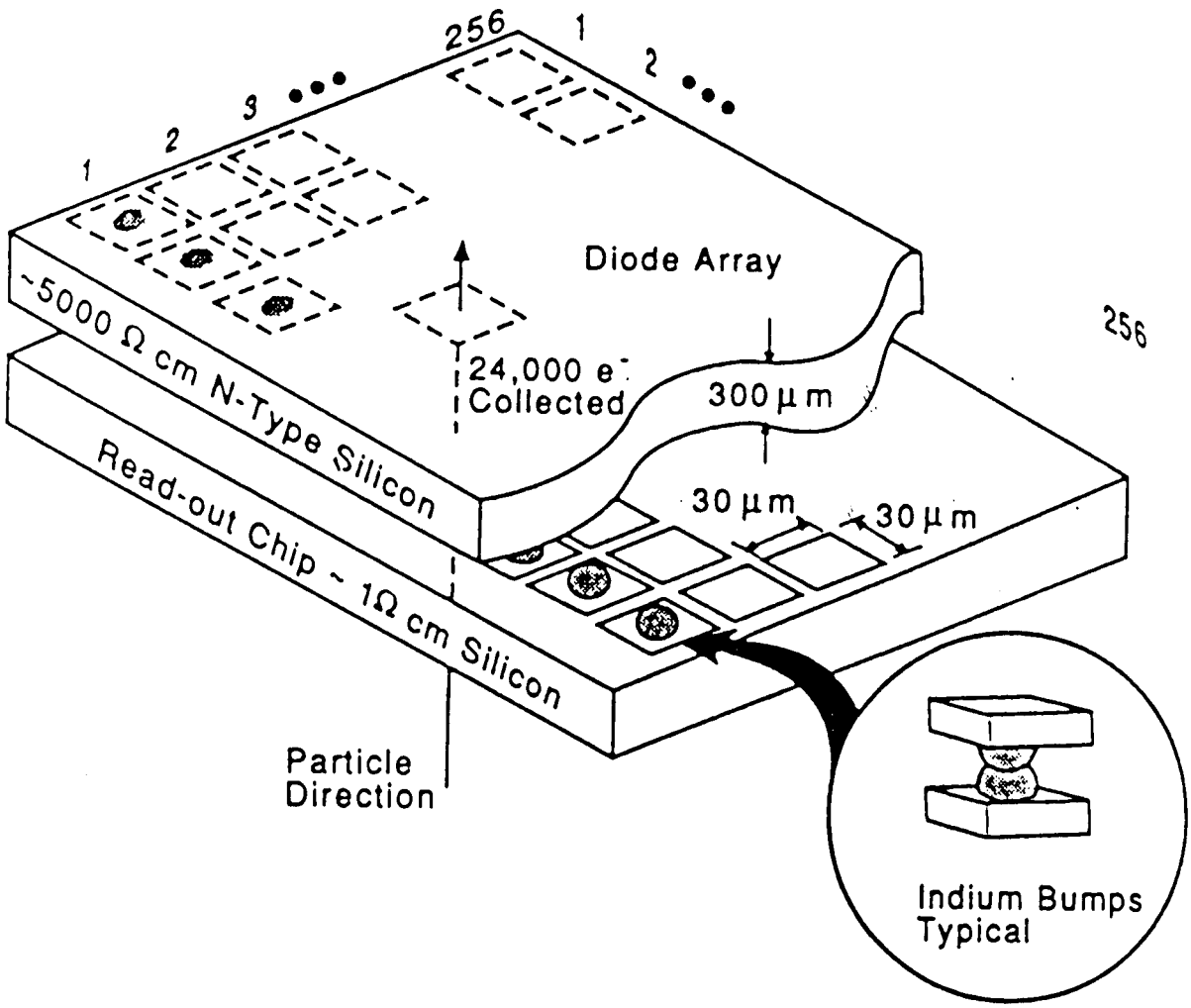
SILICON PIN DIODE ARRAY HYBRIDS FOR CHARGED PARTICLE DETECTION *

Stephen L. SHAPIRO and William M. DUNWOODIE
Stanford Linear Accelerator Center, Stanford University, Stanford, California 94309, USA

John F. ARENS and J. Garrett JERNIGAN
Space Sciences Laboratory, University of California, Berkeley, California 94720, USA

Stephen GAALEMA
Hughes Aircraft Company, Carlsbad, California 92008, USA

NIM A 275 (1989) 580-586



Silicon PIN Diode Hybrid Array used for Charged Particle Detection.

Diode Detection Layer

- Materials:
  - Silicon
  - Germanium
  - GaAs
  - CdTe

- Collection efficiency approaches 100% for high-grade materials.
- Large depth-to-width pixels are feasible.
- PSF is nearly ideal.
- Superb charge production statistics. Si: Fano Factor $\cong$ 0.1; 3.65 eV/e^--hole pair => Thousands of charges/x-ray, not tens.
- Collection speed is nsec.

CMOS Layer

Integrating:

- High instantaneous count-rate capability. Well suited for imaging.
- Flash (sub-microsecond) or push-pull mode (msec) modes.

Photon Counting:

- Discrimination used.
- Some energy resolving capability.
- Very wide dynamic range.

Hybrid Integrating and Counting.

FUNCTIONAL CHANGES ARE EASY TO IMPLEMENT

KEY PAD Attributes

- Significant problems have to be solved (rad. damage; packaging; etc.). But once solved, new detectors can be made mostly by changes in CMOS layer and external electronics.
- Problems are engineering, not new materials science.
- Most aspects of PAD technology being pushed by commercial applications.
- CMOS vendor list is growing.

PAD-Enabled Experiments

1. Laue diffraction.
2. Fine-sliced crystallography.
3. Crack propagation and destructive analysis.
4. Time-resolved diffraction.
5. Experiments which involve time structure of the ring.
6. Experiments which benefit from local in-pixel processing:
   - Local background subtraction
   - Autocorrelators
   - Local lock-in and phase sensitive methods
   - Time discriminators
   - Energy discrimination

Pixel Array Detector for Microsecond X-ray Imaging

Detector Design

Cornell University

Sol Gruner
Matt Renzi
Mark Tate
Bob Wixted (Brunswick, Maine)

Former Members

Sandor Barna	Photobit
Giusseppe Rossi	Photobit
Eric Eikenberry	PSI

Experimental Collaborators

CHESS - Cornell University

Don Bilderback
Ernie Fontes

APS - Argonne National Lab

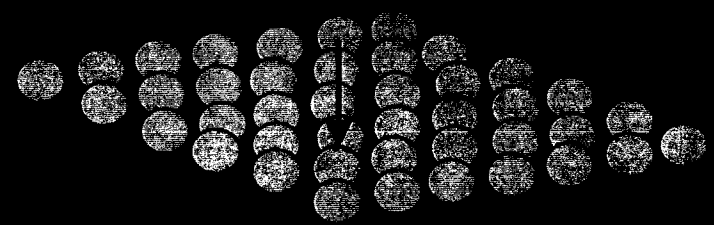
Chris Powell
Yong Yue
Armon McPherson
Ramesh Poola
Jin Wang

1463

Pixel Array Detector for Microsecond X-ray Imaging

Diode detection layer
- Fully Depleted - high resistivity
- Direct x-ray conversion
- Silicon, GaAs, CdTe

Solder Bumps
- 1 per pixel



CMOS electronics
- pixel signal processing,
- frame storage
- *Flexibility in design !*

PAD 100 x 92 pixel Prototype

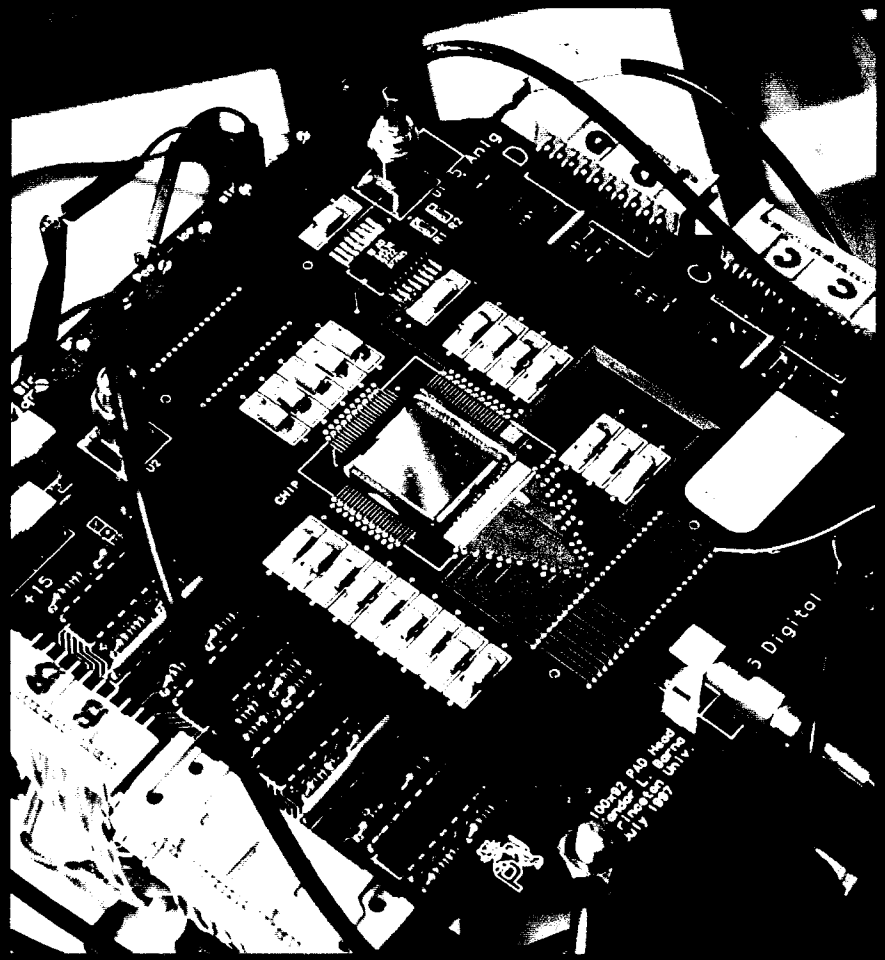
1.2 μm HP CMOS process (MOSIS)
(Linearized Capacitors)

15 x 13.8 mm^2 active area

150 μm square pixel

300 μm thick, high resistivity Si diode wafer (SINTEF)

120 μm solder bump bond
(GEC-Marconi)



Pixel Schematic

Rapid framing (SE, IR closed)

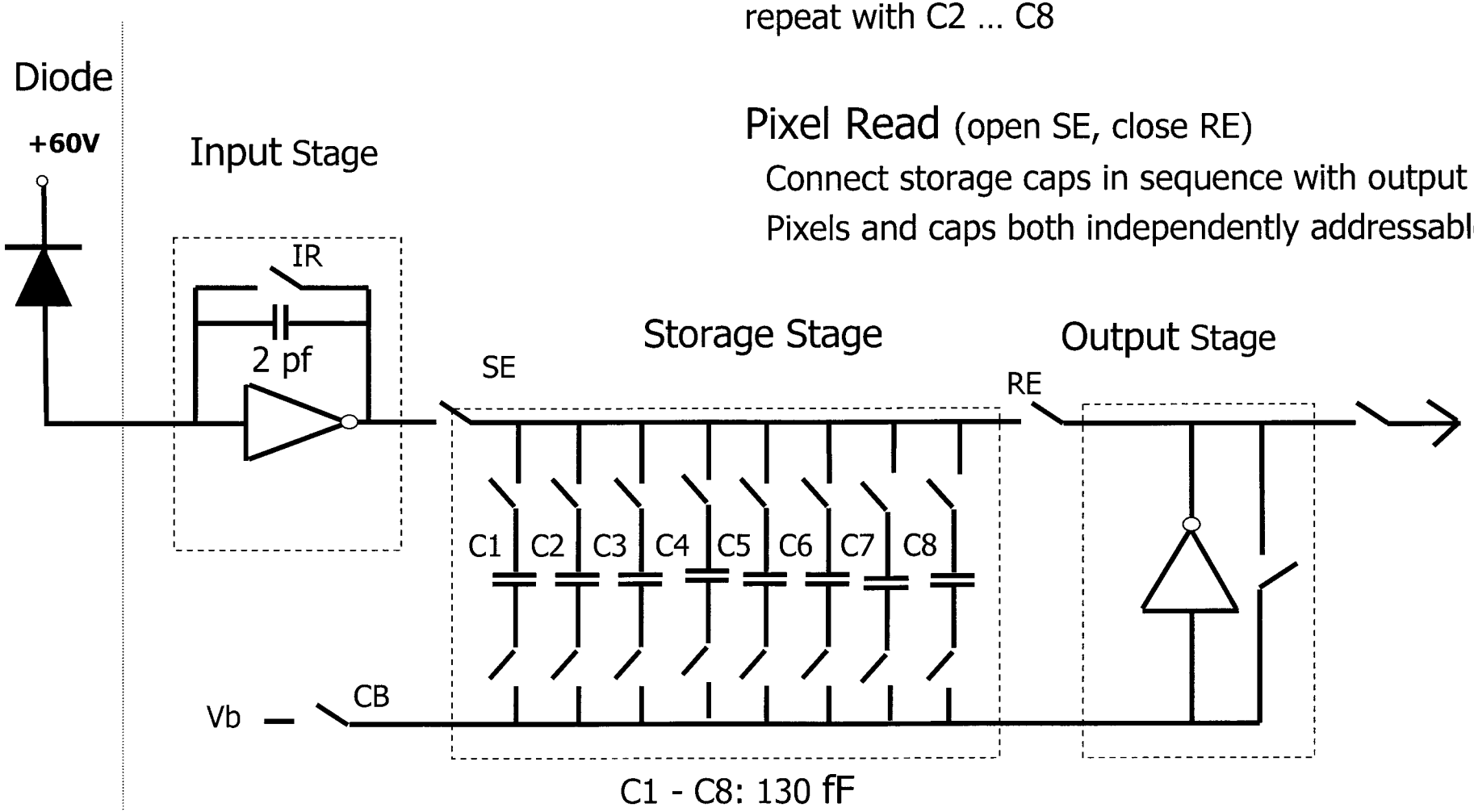
1. select storage cap C1
2. Open IR switch (Frame integration begins)
3. Deselect Storage cap (Integration ends)
4. Close IR

repeat with C2 ... C8

Pixel Read (open SE, close RE)

Connect storage caps in sequence with output

Pixels and caps both independently addressable



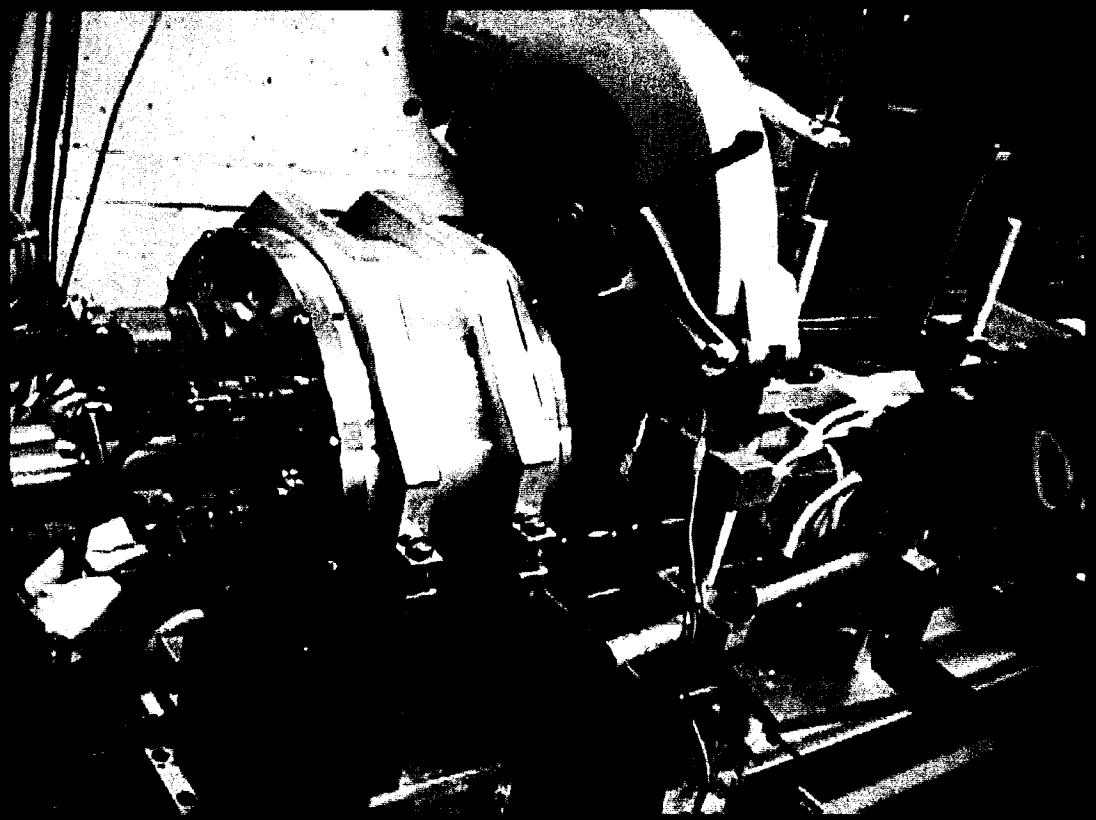
100 x 92 Prototype

Test results (8.9 keV x-rays)

• Full well capacity (x-rays)	17000
• Non-linearity (% full well)	< 0.5 %
• RMS read noise : (x-rays/pixel)	2.0 – 2.8
• Dark current (-20 C) (x-ray/pixel/s)	1.6 – 7.7
(fA/pixel)	6 – 40
• Storage capacitor leakage	0.07% / s
• PSF (@75um)	< 1%
• X-rays stopped in diode	97 %
• Minimum integration period (μs)	0.15
• Minimum deadtime between frames (μs)	0.6
• Rad damage threshold (kRad in CMOS oxide)	30
• Tolerable radiation dose (kRad)	>300

High speed imaging: CHESS

spinning saw blade - radiography



X-ray beam:

- Beamline D-1
  - (bending magnet)
- 8.9 keV (1% bandpass)
- 2 mm x 12 mm
- 10^9 x-rays/pix/s
  - (10^{12} /s in beam)

Saw blade:

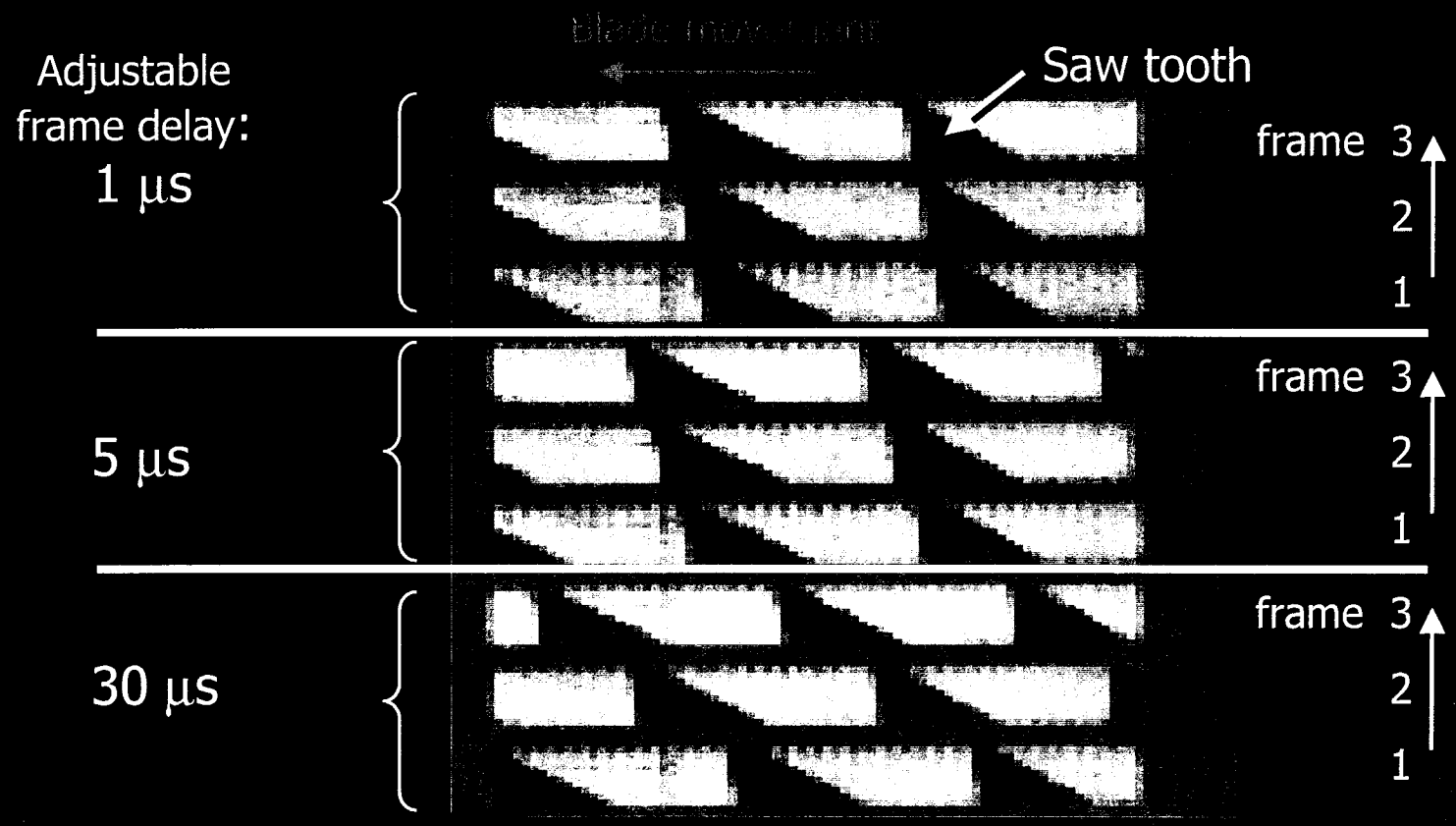
- 180 mm diameter
- 140 teeth, 2.5mm high
- 6000 RPM (teeth move 0.3 pixel/μs)

G. Rossi, *et al,* J Synchrotron Rad. (1999). **6**, 1095-1105.

Spinning saw blade: Radiography

Blade @ 6000 RPM
5 μs integration
0.3 pixel/μs motion

image 3 teeth at edge of blade
1000 x-rays/pixel/μs (8.9 keV)

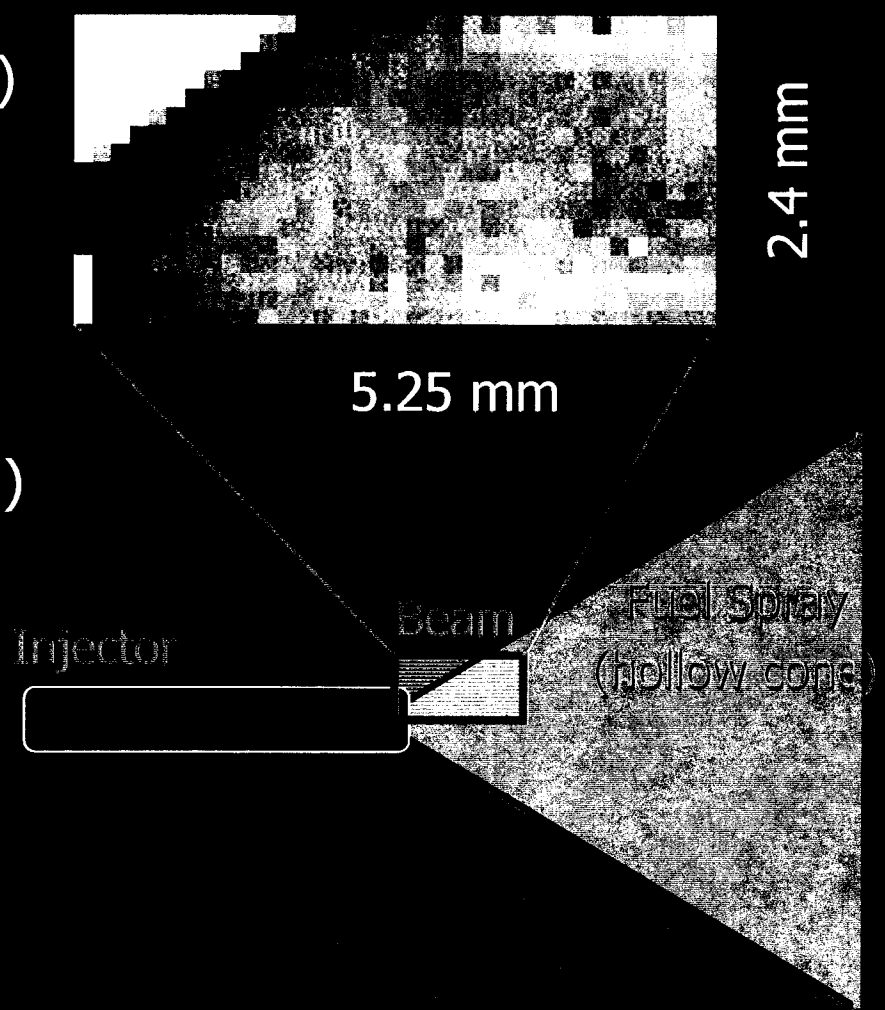


High speed imaging: APS

Fuel injector spray - radiography

x-ray beam:

- Beamline 1-BM (bending magnet)
- 6 keV (10^{-4} bandpass)
- 2.4 mm x 5.25 mm
  - (step sample to tile large area)
- 10^8 x-rays/pix/s
- 7.4 μs integration (2x ring period)



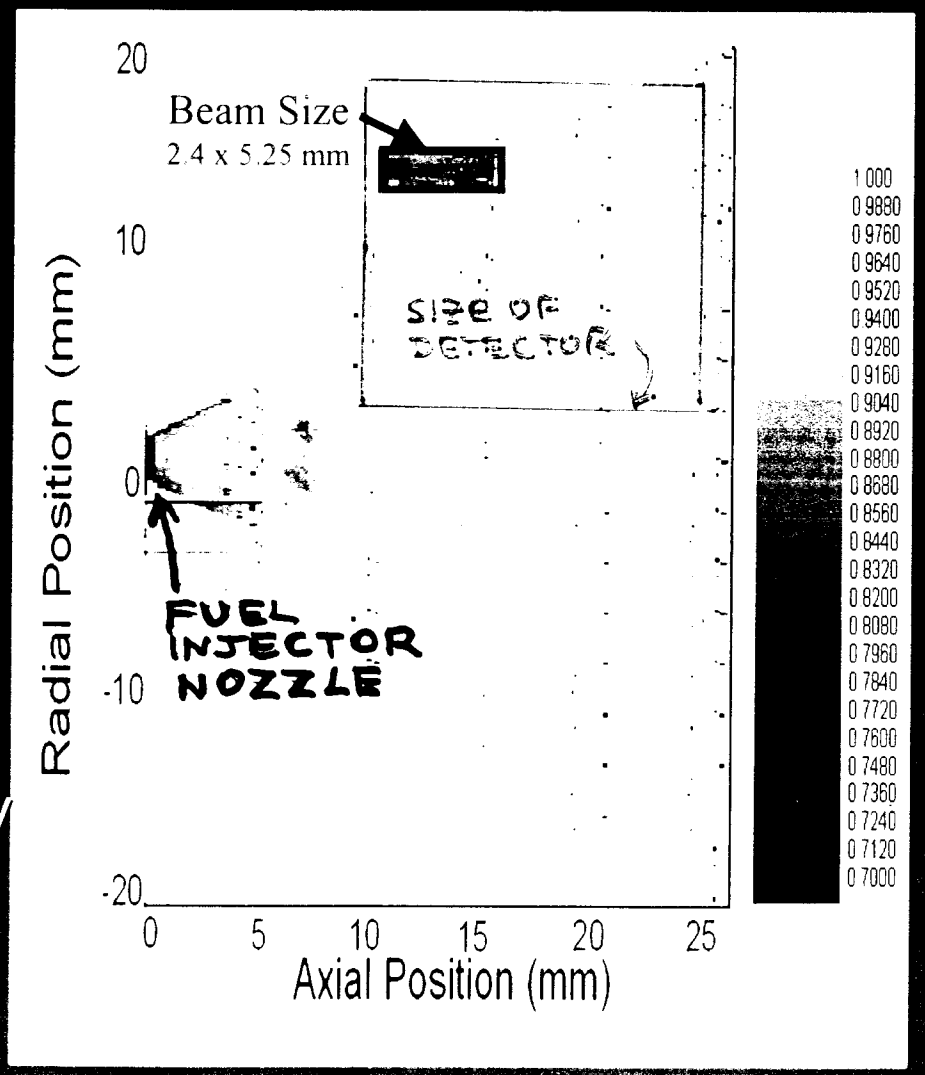
Fuel injection system:

- cesium added for x-ray contrast
- 1000 PSI gas driven
- 1 ms pulse

Fuel injector spray - radiography

2 ms time sequence (composite)

- 7.4 μs exposure time
  (44 μs between frames)
- 40 frames (5 groups of 8 frames)
- 60 beam positions
- 100-1000 x-rays/pixel/frame
- Average 100x to improve S/N
- Normalize to beam without spray



Sequence comprised of 5×10^5 images

SHOW FUEL
INJECTOR MOVIE

Enhancements to come

Radiation tolerance

- Improved shielding
- Reduction in CMOS oxide thickness / use of ring gates
  - 0.5 μm process: *pixels tested - radiation tests to be done*
  - 0.25 μm process: *in development*

Improved dynamic range *(now 17000 x-rays/pixel)*

- Digital/Analog hybrid (*e.g.* digital counter on analog overflow)
- Nonlinear integration amplifiers

Readout during integration

- Continuous millisecond framing - *0.5 μm prototype pixels tested*

Device tiling for large area coverage